Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants invention incorporating limitations from dependent claims into the independent claims.

No new issues have been raised or new matter added.

For example, support for the amendments are found in the Specification:

At paragraph 0011:

Due to the typically extremely small thickness of the dielectric layer, **formation of an interfacial layer between the dielectric layer and the bottom electrode**, as well as between the dielectric layer and the top electrode, significantly impacts EOT scaling down in the effort to achieve ever-decreasing capacitances. Top electrode interaction with thin, high-k dielectric materials has been found to adversely impact the electrical performance of MIM capacitors, including excessive junction leakage and lower breakdown voltage. Recent research indicates that the electrical performance of MIM capacitors is strongly correlated with plasma damage induced in the dielectric layer during deposition of the top electrode on the dielectric layer. This is particularly problematic with regard to dielectric layers which are fabricated using high-k dielectric materials. **Accordingly, a new and improved electrode fabrication method is needed to reduce the formation of an interfacial layer between a dielectric layer and an electrode**, as well as prevent plasma-induced damage to the dielectric layer during electrode layer

deposition, during the fabrication of an MIM capacitor on a substrate.

PREMATURE FINALITY

Applicants respectfully request withdrawal of Finality since the newly cite art not previously of record (Argawal et al. and Basceri) was not necessitated by Applicants amendments, but rather, the newly cited art represents more pertinent art to Applicants disclosed invention (i.e., Argawal shows a capacitor closer to Applicants only disclosed structural embodiment). Since Applicants are entitled to a complete search and examination of their invention including reasonably anticipated limitations that may be claimed to avoid multiple searches resulting in piecemeal examination, Applicants respectfully request withdrawal of finality of rejection to either allow entry of the present amendments to place the application in condition for allowance or for an opportunity to meaningfully amend Applicants claims to define over the newly cited art.

For example, Applicants respectfully refer Examiner to the following portions of the MPEP:

MPEP 706.07

Before final rejection is in order a clear issue should be developed between the examiner and applicant. To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant and the public, the invention as disclosed and claimed should be thoroughly searched in the first action and the references fully applied; and in reply to this action the applicant should amend with a view to avoiding all the grounds of rejection and objection. Switching from one subject matter to another in the claims presented by applicant in successive amendments, **or from one set of references to another by the examiner** in rejecting in successive actions claims of substantially the same subject matter, will alike tend to defeat attaining the goal of reaching a clearly defined issue for an early termination, i.e., either an allowance of the application or a final rejection.

MPEP 707.07(g) Piecemeal Examination
Piecemeal examination should be avoided as much as possible. The examiner ordinarily should reject each claim on all valid grounds available, avoiding, however, undue multiplication of references. (See MPEP § 904.03.)

MPEP 904.03

It is normally not enough that references be selected to meet only the terms of the claims alone, especially if only broad claims are presented; but the search should, insofar as possible, also cover all subject matter which the examiner reasonably anticipates might be incorporated into applicant's amendment. Applicants can facilitate a complete search by including, at the time of filing, claims varying

from the broadest to which they believe they are entitled to the most detailed that they would be willing to accept.

MPEP 706.07(A)

Furthermore,a second or any subsequent action on the merits in any application or patent undergoing reexamination proceedings will not be made final if it includes a rejection, on newly cited art, other than information submitted in an information disclosure statement filed under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17 (p), of any claim not amended by applicant or patent owner in spite of the fact that other claims may have been amended to require newly cited art.

A second or any subsequent action on the merits in any application or patent involved in reexamination proceedings **should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed.** See MPEP § 904 *et seq.*

Claim Rejections under 35 USC 102

1. Claims 1-4, 9-11, 13-15 stand rejected under 35 U.S.C. 102 (a)/(e) as being anticipated by Agarwal et al. (6,596,583).

Argawal disclose a process for making a thin film capacitor including a container (trench) capacitor (see Figure 9B; col 8, lines 51-58) where a tungsten nitride layer (66) is formed with an opening in dielectric layer 63 including a Ta2O5 dielectric

capacitor layer 69 and a tungsten nitride upper electrode (71). Argawal teach annealing the lower electrode tungsten nitride layer in nitrogen to convert WN to the stable W_2N phase at an anneal temperature in the range of 600-800 C (col 7, lines 44-57). Argawal teach that the lower and upper tungsten nitride electrodes may be formed by a CVD or ALD process (see col 7, lines 29-43 using organic free precursors (WF6 and NH3).

Argawal fails to disclose several key aspects of Applicants disclosed and claimed invention including those elements in **bold type**:

A method of forming an MIM capacitor to reduce interaction of high-K deposition with bottom electrode comprising:

"providing a substrate;

providing a capacitor opening in said substrate;

providing a bottom electrode in said capacitor opening;

thermally annealing said bottom electrode comprising exposing said bottom electrode to nitrogen gas while subjecting said bottom electrode to thermal processing; ;

providing a capacitor dielectric layer in said capacitor opening on said bottom electrode; and

depositing a top electrode on said capacitor dielectric layer using a plasma-free deposition process."

Argawal is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim Rejections under 35 USC 103

2. Claims 17-19 stand rejected under 35 U.S.C. Section 103(a) over Argarwal, above, and further in view of Iizuka (2002/0190294).

Applicants reiterate the comments made above with respect to Argarwal.

The further fact that Iizuka further discloses carrying out **either a plasma etchback process or a CMP process** to remove an upper portion of a bottom electrode (item 13, Fig. 7; paragraph 0087) **formed in a capacitor opening after the capacitor opening has been filled with resist** (item 14, Fig. 7) (i.e., completely different structure) does not further help Examiner in producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The

teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claims 5-8, 12, 16, and 20 stand rejected under 35 U.S.C. Section 103(a) over Argarwal in view of Iizuka, above, and further in view of Otusuki et a. (6,919,273) and Basceri et al. (2004/0046197).

Applicants reiterate the comments made above with respect to Argarwal and Iizuka.

Otusuki et al. disclose a method for forming a TiSiN film which is used as a barrier layer and/or a capacitor electrode. The TiSiN film is taught to be made by **either a thermal CVD process or a plasma CVD process** (see Abstract; col 2, lines 13-37). Otusuki et al. also teach that **Ti and TiN films have problems as barrier layers**, especially with the use of copper and that the TiSiN **barrier** layer overcomes the problems of Ti or TiN **barrier** layers (col 1, lines 43-67).

Otusuki et al. disclose several embodiments for use of the **TiSiN barrier layer** in the formation of a capacitor (see Figures 3 through Figure 8; col 3, lines 12 - col 4, line 67; col 9, lines 30 - col 10, line 32). All the embodiments in the capacitor structure of Otusuki et al., disclose forming a **planar-type capacitor structure** over an **amorphous silicon or polysilicon plug shape** (item 51, Figures 3 and 4 ; item 61, Figures 5-9), where the amorphous silicon shape (plug) in Figure 3 and 4 form the **bottom electrode** (see col 9, lines 30-43). In the embodiments in Figures 3, a **barrier layer of SiN** is formed over the bottom electrode with a TiSiN upper electrode and in Figure 4, **a TiSiN barrier layer is formed over the bottom electrode** with a **TiSiN upper electrode**. Otusuki et al. also **teach away from using a TiN film as an upper electrode** (see col 9, lines 43-49).

In other embodiments, see Figures 5-8, a **TiSiN barrier layer (item 62) is formed over a polysilicon plug** (item 61), **except for Figure 7 where a TiSiN bottom electrode** (item 67) **is formed over the polysilicon plug**. Where a **TiSiN barrier layer is formed, it is formed under a bottom electrode made of Pt or Ru** (items 63) **or over a top electrode made of Pt or Ru** (item 68, Figure 8). In one embodiment (Figure 6), **a TiSiN upper electrode (item 66) is**

formed directly on the dielectric (item 64). Otusuki et al. also teach **that Pt or Ru are preferred as electrodes and that use of the TiSiN barrier layer protects the underlying polysilicon plug** (col 10, lines 1-15).

Applicants respectfully note that Examiner erroneously asserts that Otsuki et al. teach "(at col 9, lines 1-12; lines 1-56) using a thermal CVD deposition process for forming the electrode at a low temperature of 200 - 500 °C, preferably 200 °C". However, at the reference col and line numbers teaches temperatures for cleaning a deposition chamber following TiSiN deposition (see col 9, lines 7-12). Otsuki et al. actually teach a deposition temperature for TiSiN of 400 °C to 650 °C (see col 8, lines 31-41).

Applicants also respectfully note that Examiner asserts that Basceri teaches depositing an electrode by ALD or CVD at a process temperature of about 400 °C. Applicants note that Basceri is referring to a tungsten nitride electrode in paragraph 0074 where the tungsten nitride layer is formed by a CVD process over a range of about 300 - 500 °C, preferably 400 °C. Basceri rather teaches formation of a TiN layer at a temperature of **500**

°C. to about 800 ° C. (paragraph 0070).

It is also noted by Applicants that Basceri teaches a completely different structure than Applicants or Argarwal, i.e., an MIS capacitor with the lower electrode made of hemispherical polysilicon (see Abstract) and where the capacitor dielectric is subjected to nitridization plasma annealing (see paragraph 0067).

Thus, even assuming arguendo, a proper motivation for combining the teachings of Argarwal with Otuski et al. or Basceri, such combination does not produce Applicants disclosed and claimed invention.

4. Claims 1-30 stand rejected under 35 USC Section 103(a) as being unpatentable over Otusuki et al., above, in view of Olewine et al. (2003/0067023) an Iizuka (2002/0190294).

Applicants reiterate the comments made above with respect to Otusuki et al., and Iizuka.

Applicants further note that nowhere doe Olewine teach treating a TiN electrode with nitrogen.

On the other hand, Olewine et al. disclose a significantly different **serpentine capacitor structure** (see Figure 1) where the **bottom electrode** (see item 2, Figure 30) **is protruding above a substrate** formed from a block of conductor material such as **aluminum or copper** (see paragraph 0034) which includes an overlying conductive material (item 34) that functions as an etch stop layer **disclosed to be TiN** (paragraph 0047, 0048), a capacitor dielectric (item 36) on the TiN and an upper electrode (38) (which may be TiN) on the capacitor dielectric where the capacitor dielectric and the upper electrode are patterned **and plasma etched together** (paragraph 0036, paragraph 0070-0078) **to stop on the bottom TiN layer.** Olewine et al. also disclose **plasma annealing** the dielectric layer following deposition (paragraph 0062). Olewine et al. also disclose **PVD reactive sputtering to form the upper TIN electrode** (paragraph 0064).

Olewine et al. also disclose carrying out an **ammonia plasma treatment** of the bottom electrode prior to deposition of the capacitor dielectric to remove oxidation and to inhibit formation of TiO (paragraph 0055, 0056).

The fact that Iizuka further discloses carrying out **either a plasma etchback process or a CMP process** to remove an upper portion of a bottom electrode (item 13, Fig. 7; paragraph 0087) formed in a capacitor opening after the capacitor opening has been filled with resist (item 14, Fig. 7) does not further help Examiner in making out a *prima facie* case of obviousness.

For example, Iizuka also teaches that following CMP the **resist filling the capacitor must be removed by plasma etching and that damage to the lower electrode occurs** (see paragraphs 0088, 0089). To overcome this problem, Iizuka teach forming the lower electrode, the capacitor dielectric and the upper electrode in the same ALD machine (paragraph 0090, 0100, Fig. 9I) **which is then followed** by **either a CMP process or a plasma etchback process** to remove surface portions of the capacitor structure (Fig 9J; paragraph 0112).

There appears to be no motivation to combine the teachings of the disparate capacitor structures and method for forming the same of Iizuka, Otusuki et al. and Olewine et al., which all teach significantly different capacitor structures formed by completely different methods. For example, the capacitor

structure of Iizuka when formed in the same ALD machine is never exposed to air and therefore would not need the ammonia plasma treatment in the method of Olewine et al.

Nevertheless, even assuming *arguendo*, a proper motivation for combination such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

Conclusion

The multiplicity of cited references, either alone or in combination, do not produce Applicants disclosed and claimed invention and therefore fail to produce Applicants invention and therefore fail to make out a *prima facie* case of anticipation oor bviousness with respect to Applicants independent and dependent claims.

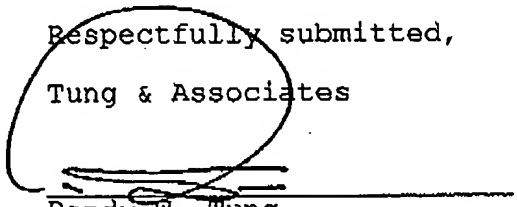
The claims have been amended to clarify Applicants disclosed and claimed invention.

Based on the foregoing, Applicants respectfully request withdrawal of Finality and reconsideration of Applicants claims and submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates



Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040